

green, blue, cyan, magenta, yellow, black or white). "Off" pixels can be made "transparent", displaying the external video instead of black. A character can also be displayed "inverse", in which the "on" and "off" pixels are reversed. It is also possible to mix transparent mode with inverse mode so that "on" pixels display the external video.

PLD U111 provides timing signals required to scan the characters out to the display. It contains an up-counter clocked by PIXCLKB, which divides the active horizontal scan time into 64 time slots (columns). It also contains a vertical counter clocked by VLTC from the vertical RAM circuit (described below), which divides the raster into 24 rows. During the first half of each horizontal time slot, U111 generates a column address (CG0-CG5) and a row address (CG6-CG11), which together specify one of the screen locations. CG12 is low to address the lower half of RAM space. In response to this address, RAMs U97 and U98 each output a byte. One byte (the attribute byte) is clocked into latch U89 using FONT-CLK. The other byte is clocked into latch U91.

During the second half of the horizontal time slot, the data in U91 is fed back to the RAMs on CG4-CG11. In addition, CG12 goes high to address the upper half of the RAM space. Together, these bits address one of the character bitmaps. Address bits CG0-CG3 from the vertical RAM circuit (described below) specify which line of pixels in the bitmap will be displayed on the current scan line. In response to this new address, RAMs U97 and U98 each output another byte. These are loaded into shift registers U88 and U99 using LOADSHIFT*. At the same moment, the attribute byte in U89 is latched into U90. This ensures that a character's attributes take effect at the same time its pixels are shifted out to the display.

3.3.1.1 Vertical RAM Circuit

The vertical RAM circuit is composed of a 12-bit counter (U114), a RAM (U102), a latch (U101), and several buffers (U100, U112, U113, U115, U116). The counter generates an address for the RAM which is incremented every scan line. Therefore, one unique byte is output from the RAM for every scan line in the raster. The RAM is loaded by the 68000 microprocessor on the MSB of its data bus (D8-D15).

The four most significant bits from the RAM are multiplexed onto address lines CG0-CG3 by buffer U100 during the second half of a horizontal time slot. These address bits select which of the sixteen bytes in a character's bitmap will be displayed on a given scan line in the raster. The bits in each byte are loaded by the 68000 with values that ensure a uniform appearance of the characters regardless of the number of scan lines in the raster. If there are more scan lines in the raster than the number of rows times the number of bytes in each bitmap ($24 \times 16 = 384$), then some bytes are repeated over several scan lines. This is done to preserve the size and on-screen position of the text rows. For the same reason, if there are less than 384 scan lines in the raster, some bytes are omitted.

The four least significant bits from RAM U102 are clocked into latch U101. As the raster lines are scanned down the screen, the individual bits create digital waveforms. The waveform VLTC is a clock signal which increments the row counter in U111 once for each row of text. VBL is the vertical blanking waveform, which is affected by user-settings for top blanking and bottom blanking. The screen is blanked when VBL is high. The waveform MIDV marks the exact middle of the raster. It is used by the grayscale test pattern circuit.